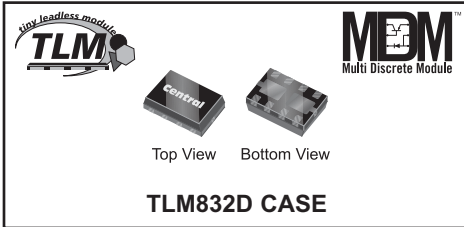


CTLM7110-M832D
MULTI DISCRETE MODULE™
SURFACE MOUNT N-CHANNEL
ENHANCEMENT-MODE SILICON MOSFET
AND
LOW V_F SILICON SCHOTTKY RECTIFIER



www.centrasemi.com



• Device is **Halogen Free** by design

APPLICATIONS

- Load Power Switches
- DC - DC Converters
- LCD Backlighting
- Battery powered portable devices including Cell Phones, Digital Cameras, Pagers, PDAs, Notebook PCs, etc.

MAXIMUM RATINGS - CASE: ($T_A=25^\circ\text{C}$)

Power Dissipation (Note 1)
 Operating and Storage Junction Temperature
 Thermal Resistance

MAXIMUM RATINGS - Q1: ($T_A=25^\circ\text{C}$)

Drain-Source Voltage
 Gate-Source Voltage
 Continuous Drain Current (Steady State)
 Maximum Pulsed Drain Current, $t_p=10\mu\text{s}$

MAXIMUM RATINGS - D1: ($T_A=25^\circ\text{C}$)

Peak Repetitive Reverse Voltage
 Continuous Forward Current
 Peak Repetitive Forward Current, $t_p \leq 1.0\text{ms}$
 Peak Forward Surge Current, $t_p=8.0\text{ms}$

ELECTRICAL CHARACTERISTICS - Q1: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{GSSF}, I_{GSSR}	$V_{GS}=8.0\text{V}, V_{DS}=0$			10	μA
I_{DSS}	$V_{DS}=20\text{V}, V_{GS}=0$			10	μA
BV_{DSS}	$V_{GS}=0, I_D=250\mu\text{A}$	20			V
$V_{GS(th)}$	$V_{DS}=10\text{V}, I_D=1.0\text{mA}$	0.5		1.2	V
V_{SD}	$V_{GS}=0, I_S=1.0\text{A}$			1.1	V
$r_{DS(ON)}$	$V_{GS}=4.5\text{V}, I_D=0.5\text{A}$		0.075	0.10	Ω
$r_{DS(ON)}$	$V_{GS}=2.5\text{V}, I_D=0.5\text{A}$		0.10	0.14	Ω
$r_{DS(ON)}$	$V_{GS}=1.5\text{V}, I_D=0.1\text{A}$		0.17	0.25	Ω
$Q_g(\text{tot})$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=1.0\text{A}$		2.4		nC
Q_{gs}	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=1.0\text{A}$		0.25		nC
Q_{gd}	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=1.0\text{A}$		0.65		nC
g_{FS}	$V_{DS}=10\text{V}, I_D=0.5\text{A}$		4.2		S

Notes: (1) FR-4 Epoxy PCB with copper mounting pad area of 54mm².

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLM7110-M832D consists of an N-Channel Enhancement-mode MOSFET and a Low V_F Schottky Rectifier. Packaged in a small, thermally efficient, leadless 3x2mm surface mount case, it is designed for applications where small size, operational efficiency, and low energy consumption are the prime requirements.

MARKING CODE: CFL

FEATURES

- Dual Chip Device
- High Current (1.0A) MOSFET and Schottky Rectifier
- Low $r_{DS(ON)}$: 0.25 Ω MAX @ $V_{GS}=1.5\text{V}$
- Low V_F Schottky Rectifier (550mV @ 1.0A MAX)
- ESD Protection up to 2KV
- Small TLM 3x2mm Leadless Surface Mount Package
- Complementary Device: CTLM8110-M832D

SYMBOL		UNITS
P_D	1.65	W
T_J, T_{stg}	-65 to +150	$^\circ\text{C}$
θ_{JA}	76	$^\circ\text{C/W}$
V_{DS}	20	V
V_{GS}	8.0	V
I_D	1.0	A
I_{DM}	4.0	A
V_{RRM}	40	V
I_F	1.0	A
I_{FRM}	3.5	A
I_{FSM}	10	A

R2 (2-August 2011)

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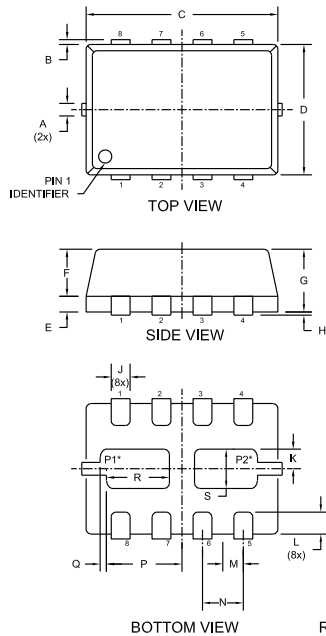
ELECTRICAL CHARACTERISTICS - Q1 - Continued: ($T_A=25^\circ\text{C}$)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
C_{rss}	$V_{DS}=10\text{V}$, $V_{GS}=0$, $f=1.0\text{MHz}$		45		pF
C_{iss}	$V_{DS}=10\text{V}$, $V_{GS}=0$, $f=1.0\text{MHz}$		220		pF
C_{oss}	$V_{DS}=10\text{V}$, $V_{GS}=0$, $f=1.0\text{MHz}$		120		pF
t_{on}	$V_{DD}=10\text{V}$, $V_{GS}=5.0\text{V}$, $I_D=0.5\text{A}$		25		ns
t_{off}	$V_{DD}=10\text{V}$, $V_{GS}=5.0\text{V}$, $I_D=0.5\text{A}$		140		ns

ELECTRICAL CHARACTERISTICS - D1: ($T_A=25^\circ\text{C}$)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_R	$V_R=5.0\text{V}$			10	μA
I_R	$V_R=8.0\text{V}$			20	μA
I_R	$V_R=15\text{V}$			50	μA
BV_R	$I_R=100\mu\text{A}$	40			V
V_F	$I_F=10\text{mA}$			0.29	V
V_F	$I_F=100\text{mA}$			0.36	V
V_F	$I_F=500\text{mA}$			0.45	V
V_F	$I_F=1.0\text{A}$			0.55	V
C_J	$V_R=4.0\text{V}$, $f=1.0\text{MHz}$		50		pF

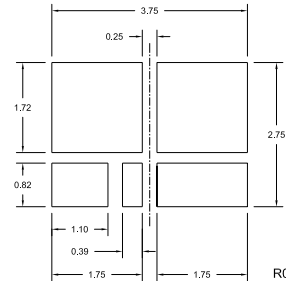
TLM832D CASE - MECHANICAL OUTLINE



SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.007	0.012	0.170	0.300
B	-	0.005	-	0.125
C	0.114	0.122	2.900	3.100
D	0.075	0.083	1.900	2.100
E	0.006	0.010	0.150	0.250
F	0.026	0.030	0.650	0.750
G	0.031	0.039	0.800	1.000
H	0.000	0.002	0.000	0.050
J	0.009	0.013	0.240	0.340
K	0.006	0.014	0.160	0.360
L	0.008	0.018	0.200	0.450
M	0.013		0.325	
N	0.026		0.650	
P	0.040	0.048	1.010	1.210
Q	0.004		0.100	
R	0.032	0.040	0.820	1.020
S	0.017	0.025	0.430	0.630

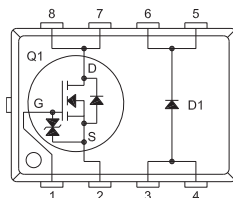
TLM832D (REV: R2)

SUGGESTED MOUNTING PADS
 For Maximum Power Dissipation
 (Dimensions in mm)



For standard mounting refer
 to TLM832D Package Details

PIN CONFIGURATION



LEAD CODE:

- 1) Gate Q1 5) Cathode D1
- 2) Source Q1 6) Cathode D1
- 3) Anode D1 7) Drain Q1
- 4) Anode D1 8) Drain Q1

MARKING CODE: CFL

* Note:
 - Exposed pad P1 common to pins 7 and 8
 - Exposed pad P2 common to pins 5 and 6

R2 (2-August 2011)